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Description

[SILICON DIOXIDE REMOVING METHOD]

BACKGROUND OF INVENTION

[0001] Technical Field

[0002] The present invention relates generally to semiconductor fabrication, and more particularly, to a silicon dioxide removing method useful for fabricating a hetero-junction bipolar transistor (HBT).

[0003] Related Art

[0004] Removal of silicon dioxide (i.e., oxide) is problematic relative to a variety of semiconductor fabrication processes such as fabrication of a raised source/drain complementary metal-oxide semiconductor (CMOS), silicon-on-insulator (SOI) devices, field-effect transistor (FET) gate oxide generation, etc. One illustrative process in which oxide residuals cause significant problems is the fabrication of silicon (Si) NPN and silicon-germanium (SiGe) HBTs. In this application, a thin oxide emitter-base interface traditionally separates the arsenic doped emitter

polysilicon from the boron doped single crystal SiGe base. Referring to FIG. 1, a HBT 2 having a thin oxide emitter-base interface 4 is shown. Oxide interface 4 is known to control the holes re-injected back into emitter 6 as base 8 current, and the out-diffusion of arsenic from emitter 6 polysilicon into single crystal base 8. The arsenic out-diffusion forms the actual emitter-base junction in the single crystal silicon base 8. This oxide interface 4 is currently grown using a low temperature rapid thermal oxidation (RTO) process.

[0005] Problems related to oxide interface 4 arise relative to reducing emitter resistance (Re) of NPN transistors in conventional silicon-germanium (SiGe) technology. Reducing Re is advantageous because high Re causes collector current to roll off quickly. A thin oxide interface 4 (FIG. 1), described above, and the non-self aligned polysilicon emitter, are known to contribute significantly to Re. One approach to address this problem is to provide deposition of in-situ doped (ISD) arsenic amorphous silicon to form the emitter without an oxide interface. In this case, the amorphous region re-crystalizes off seed silicon of the base because there is no interfacial oxide. This approach reduces Re by as much as five times, and improves high

performance HBT device cutoff frequency by approximately 6 GHz. Unfortunately, this approach is unreliable. First, some wafers within a lot exhibit high Re compared to the specified amount using this approach. Second, certain wafers exhibit high trans-wafer variation of Re using this approach. Some of the high Re wafers are also accompanied by lower NPN yield due to interference of oxide residuals at the interface, which causes local strain field distortion and misaligned dislocations. Accordingly, the ISD approach's unreliability makes it difficult for process control during manufacturing.

[0006] In view of the foregoing, there is a need in the art for an improved semiconductor cleaning method for removing oxide residuals.

SUMMARY OF INVENTION

[0007] The invention includes a method for removing silicon dioxide residuals. from a surface of a semiconductor The method includes reacting a portion of a silicon dioxide layer (i.e., oxide) to form a reaction product layer, removing the reaction product layer and annealing the surface to remove oxide residuals. The method finds application in a variety of semiconductor fabrication processes. One example is the fabrication of an improved hetero-junction

bipolar transistor (HBT) and an in-situ deposition (ISD) arsenic process for generating the HBT without an oxide interface at the emitter-base. In this case, the invention provides reduced Re, increased NPN yield and a more uniform Re distribution across a wafer without sacrificing any other device performance characteristics. In addition, the invention provides an improved NPN emitter process window to maintain a stable and manufacturable HBT process. The inventive method may also be implemented to form a silicon-to-silicon interface without an oxide interface.

[0008] A first aspect of the invention is directed to a method of removing silicon dioxide from a surface of a semiconductor, the method comprising the steps of: a) reacting the silicon dioxide to form a reaction product on the surface; b) removing the reaction product from the surface; and c) annealing the surface.

[0009] A second aspect of the invention is directed to a method of forming a vertical bipolar transistor having a single crystal base formed on a substrate, the method comprising the steps of: a) forming a silicon dioxide layer and a dielectric layer on the base; b) forming an emitter window in the dielectric layer over the base to expose a portion of

the silicon dioxide layer; c) reacting the portion of the silicon dioxide layer to form a reaction product layer; d) removing the reaction product layer from the emitter window to expose a surface of a portion of the base; e) annealing the substrate and f) forming a single crystal emitter on the exposed surface of the base.

[0010] A third aspect of the invention is directed to a method of forming an interface between a first single crystal silicon layer and a second single crystal silicon layer, the method comprising the steps of: a) forming a silicon dioxide layer on the second single crystal silicon layer; b) reacting at least a portion of the silicon dioxide layer to form a reaction product layer; c) removing the reaction product layer to expose a surface of the second single crystal silicon layer; d) annealing the surface and e) forming the first single crystal silicon layer on the surface of the second single crystal silicon layer.

[0011] The foregoing and other features of the invention will be apparent from the following more particular description of embodiments of the invention.

Brief Description of Drawings

[0012] The embodiments of this invention will be described in detail, with reference to the following figures, wherein like

designations denote like elements, and wherein:

[0013] FIG. 1 shows a prior art HBT with a thin oxide emitter-base interface.

[0014] FIGS. 2-5 show a method for removing silicon dioxide according to the invention.

[0015] FIGS. 6-10 show a method of forming a vertical HBT using the method of FIGS. 2-5.

[0016] FIGS. 11-14 show a method of forming an interface between a first single crystal silicon layer and a second single crystal silicon layer using the method of FIGS. 2-5.

DETAILED DESCRIPTION

[0017] A method for removing silicon dioxide will now be described. In a first step of the method, as shown in FIGS. 2-3, a silicon dioxide (hereinafter "oxide") layer 10 (FIG. 2) that is present on a surface 12 of a semiconductor device 14, e.g., a substrate, is reacted to form a reaction product 16 (FIG. 3), as described in U.S. Patent No. 5,282,925, which is hereby incorporated by reference. In one embodiment, oxide layer 10 is reacted by exposure to a vapor phase etch 20 (FIG. 2) comprising hydrogen fluoride and ammonia gas. In another embodiment, vapor phase etch 20 comprises ammonia bifluoride. The conditions and concentrations of material may vary according to specific

applications. In one embodiment, the reaction occurs at room temperature and approximately 5 mTorr. Reaction product 16 (FIG. 3) includes etched oxide and reactants and combinations thereof.

[0018] Next, as shown in FIG. 4, the reaction product is removed. In one embodiment, removal is accomplished by evaporating the reaction product from surface 12. Evaporation may be made, for example, by heating the substrate to approximately 100 °C, as described in U.S. Patent No. 5,282,925. In another embodiment, removal may be accomplished by rinsing surface 12 with water ($H_2 0$), i.e., reaction product 16 is water soluble.

[0019] As shown in FIG. 5, the next step includes annealing surface 12, e.g., substrate, in an environment 22 such as, for example, a vacuum, a reducing atmosphere, or an inert atmosphere, to remove any remaining oxide 24 not removed during the removing step. In one embodiment, the reducing atmosphere comprises hydrogen (H_2).

[0020] The resulting surface 12 is substantially free of silicon dioxide, e.g., the oxygen dose at the surface is less than $2 \times 10^{14} /cm^2$.

[0021] Example Application 1:One example application of the above-described method is use in fabrication of a vertical

HBT. According to the first embodiment, in a first step, shown in FIG. 6, a silicon dioxide layer 110 and a dielectric layer 111, e.g., silicon nitride, are formed on a single crystal base 130 of, for example, silicon (Si) or silicon-germanium (SiGe). FIG. 6 also shows other underlying structure such as substrate 132 including shallow trench isolations 134 and NPN intrinsic region 136. Next, as shown in FIG. 7, an emitter window 138 is formed in silicon nitride layer 111 over base 130 to expose a portion 140 of silicon dioxide layer 110.

[0022] Next, as shown in FIG. 8, oxide layer 110 is reacted to form a reaction product 116, as discussed above. That is, oxide layer 110 is reacted by exposure to a vapor phase etch 120 using, for example, hydrogen fluoride and ammonia, or ammonia bifluoride. Again, the conditions and concentrations of material may vary according to specific applications. In one embodiment, the reaction occurs at room temperature and approximately 5 mTorr. Reaction product 116 includes etched oxide and reactants and combinations thereof.

[0023] As shown in FIG. 9, the reaction product is removed, as described above, to expose a surface 112 of base 130 (excepting remaining oxide 124). As also shown in FIG. 9,

the next step includes annealing surface 112, e.g., substrate, in , for example, a reducing atmosphere 120 to remove any remaining oxide 124. In one embodiment, reducing atmosphere 120 comprises hydrogen (H2). Further, the process temperature is high enough to remove any remaining oxide 124 yet low enough so as to not disturb, for example, a boron implant (not shown) in single crystal base 130. A preferred process temperature range to satisfy these conditions is from approximately 700°C to approximately 800°C, and occur for approximately 5-15 seconds.

[0024] Finally, as shown in FIG. 10, a single crystal emitter 150 may be formed on exposed surface 112 of base 130 to complete HBT 160. In one embodiment, this step is provided by an ISD 152 of arsenic (As) doped silicon. HBT 160 formed with this embodiment show improved AC performance. For example, single crystal ISD (As) doped emitter devices have exhibited an Re significantly less than implanted polysilicon emitter devices.

[0025] The resulting HBT 160 does not contain any oxide interface at the emitter-base interface 162. As a result, HBT 160 exhibits improved emitter resistance (Re). The above-described process also provides for reliable reproduction

of a low Re HBT within a lot and across a wafer. Another advantage is that emitter film crystallinity is improved with fewer defects, which enhances NPN yield by reducing defects penetrating through the emitter to the collector. Improved yields of approximately 15% have been attained using the above-described method. Further, NPN DC parameter characterization, such as tighter transistor current gain (Beta) distribution, increased emitter base junction reverse breakdown voltage (Bvebo) and decreased emitter base junction capacitance (Ceb), and defects such as voids or misfit dislocation are reduced in the emitter region, which improves dopant distribution and dopant diffusion caused by the defects. Another advantage of the above-described method is that the removing, annealing and emitter forming steps may occur in the same process tool, which reduces process complexity. In addition, the removing, annealing and emitter forming step may be performed in an oxygen-free ambient to prevent formation of a native oxide layer.

[0026] Example Application 2:In another illustrative application, the above-described method may be implemented to form an interface between a first single crystal silicon layer and a second single crystal silicon layer. In this ap-

plication, the method may include: a) forming a silicon dioxide layer 210 on single crystal silicon layer 200, as shown in FIG. 11; b) reacting at least a portion of the silicon dioxide layer 210 to form a reaction product layer 216, as shown in FIG. 12; c) removing reaction product layer 216 to expose a surface 212 of single crystal silicon layer 200; d) annealing in, for example, a reducing atmosphere 222; and e) forming a single crystal silicon layer 202 on surface 212 of single crystal silicon layer 200, as shown in FIG. 14.

[0027] While the inventive method has been described in detail relative to illustrative applications including a method of forming a vertical HBT and a method forming an interface between a single crystal silicon layers, it should be recognized that the invention is applicable to practically any semiconductor fabrication process in which oxide is removed. The invention thus finds applicability in other fabrication processes such as those for a raised source/drain in CMOS, SOI devices, FET gate oxide, etc.

[0028] While this invention has been described in conjunction with the specific embodiments outlined above, it is evident that many alternatives, modifications and variations will be apparent to those skilled in the art. Accordingly,

the embodiments of the invention as set forth above are intended to be illustrative, not limiting. Various changes may be made without departing from the spirit and scope of the invention as defined in the following claims.